

Examiner's characterization of the Zhao and Kato references as described below.

Claim 4 recites, *inter alia*, "selectively etching said first insulating layer with plasma, using said selectively-etched second insulating layer as a mask pattern". Therefore, it is possible to obtain a semiconductor device wherein the first insulating layer containing carbon contacts the second insulating layer comprising silicon, carbon, and nitrogen between the wiring layers. As a result, the following effects, for example, may be obtained:

- a) the adhesion between the first and second insulating layers is improved to inhibit peeling;
- b) the second insulating layer, as the mask pattern for etching the first insulating layer with plasma, has a higher etch selectivity than those of conventional layers; and
- c) the second insulating layer, comprising silicon, carbon, and nitrogen has a lower dielectric constant than that of an insulating layer comprising silicon and nitrogen or an insulating layer comprising silicon and carbon.

Therefore, it is possible to improve the reliability of the semiconductor device while considering the acceleration of the same.

None of the cited references disclose such a second insulating layer, nor do they suggest that the SiCN film is used as an insulating layer forming a part of a semiconductor device, as well as a mask pattern for etching an underlying insulating layer of the same.

More specifically, the SiCN film of Kato is not an interlayer-film of a semiconductor device and is not a mask pattern for etching an underlying layer with

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

plasma. The SiCN film of Kato is used for a radiation-transmitting substrate (not a mask pattern) of an independent mask-system for lithography using X-rays or the like. Accordingly, the SiCN film of Kato has nothing to do with the second insulating layer of the present invention.

Therefore, one of ordinary skill would not be motivated to apply the SiCN film of Kato to an interlayer-film that serves both as an insulating layer of a semiconductor device and a mask-pattern for forming a part of the semiconductor device to obtain the above described results achievable by the presently claimed invention.

In addition, the Examiner rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over Zhao in view of Kato as applied to claims 4-8 and further in view of Chen et al. Claim 9 depends from claim 4 and is believed to be allowable for at least the reasons stated above.

Applicant believes claim 4 is now in condition for allowance and respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

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By: 

David W. Hill
Reg. No. 28,220

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

APPENDIX TO AMENDMENT OF FEBRUARY 12, 2002

Version with Markings to Show Changes Made

Amendments to the Claims

4. (Amended) A method of manufacturing a semiconductor device, said method comprising the steps of:

forming a wiring layer on a semiconductor substrate[, on which] having an active region [is] formed thereon;

forming a first insulating layer comprising silicon, carbon and nitrogen on said first insulating layer;

selectively etching said second insulating layer until the surface of said first insulating layer is partially exposed,

selectively etching said first insulating layer with plasma, using said selectively-etched second insulating layer as a mask pattern; and

forming a new wiring layer on said second insulating layer after selectively etching said first insulating layer.

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HENDERSON
FARABOW
GARRETT &
DUNNER LLP

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Washington, DC 20005
202.408.4000
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